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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,919	08/20/2003	Yoshitaro Yazaki	01-244-DIV	5017

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EXAMINER	
MAYES, MELVIN C	

ART UNIT	PAPER NUMBER
1734	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,919	YAZAKI ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-23 and 27-39* is/are rejected.

7)☒ Claim(s) *24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/024,470.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/20/03,12/16/03,6/22/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

(1)

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

(2)

Claims 30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 30 and 31 recite the limitation "the relatively fine particles." There is insufficient antecedent basis for this limitation in the claim.

Claims 30 and 31 recite the limitation "the interlayer **connecting** material." There is insufficient antecedent basis for this limitation in the claim. The claims should read "interlayer conducting material."

Double Patenting

(3)

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

(4)

Claims 11, 12 and 15 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 9, 11, 12 and 14 of copending Application No. 10/662368. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Application No. 10/662368 claims a fabrication method for a printed wiring board comprising packing an interlayer connecting material in a via-hole formed in an insulator film and interconnecting a plurality of conductor patterns with a unified conductive compound formed by hot-pressing the interlayer connection material in the via-hole between conductor patterns, wherein the interlayer connecting material contains metal particles including first metal particles and second metal particles having a higher melting point than the heating temperature for interconnecting layers and the conductor patterns are interconnected by a unified conductive compound and a solid phase diffusion formed between the fist metal and the conductor pattern through the hot-press, wherein the first particles are tin included in an amount between 20 wt% and 80 wt%.

It would have been obvious to one ordinary skill in the art to interconnected conductor patterns by stacking layers of insulator film for hot-pressing

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

(5)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

(6)

Claims 11-18, 20-22, 27, 32 and 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 0 793 405.

EP 0 793 405 discloses a method of making a multilayer circuit board comprising: providing dielectric layers, such as polyimide film, having copper cladding; forming vias in the dielectric layers, forming copper circuitry from the copper cladding; filling the vias with a via fill material; laminating dielectric layers; and heating under pressure to form an intermetallic compound in the vias. The first component in the via fill material is a relatively high melting particulate phase material, such as copper, nickel gold or silver, of particle size of 0.5-15 microns. The second component in the via fill material is a low melting material such as tin or tin alloy or indium of particle size of 1-150 microns. The via fill material further comprises one or more resins and solvent. When the via fill material is of copper and tin, the laminate is heated to between 180°C and 325°C and forms a copper-tin intermetallic compound. EP '405 discloses mixing 30.3 grams of tin/lead particles and 60.6 grams of copper particles for making a via fill material and discloses heating under a pressure of 250 psi (1.7 MPa) (pgs. 1-14).

By heat-pressing at 180°C and 325°C a laminate containing vias filled with a material of either tin or indium particles and either copper, nickel gold or silver particles and containing copper circuitry to form a copper-tin intermetallic compound in the vias, a solid conductive material is obviously formed in the vias including a unified conductive layer and solid phase diffusion layer of either tin or indium and the copper, as claimed.

Further by filling the vias with tin or indium of particle size in the range of 1-150 microns and copper of particle size in the range of 0.5-15 microns, such as 0.5 microns (500 nm), the vias

are obviously filled with a metal of relatively large particles and with a metal of relatively fine particles in the range of 1-500 nm, as claimed in Claim 32, and a solid conductive material is obviously formed in the through-holes including a unified conductive layer and solid phase diffusion layer of tin or indium and the copper, as claimed in Claim 28 and 29.

(7)

Claims 23 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP '405 as applied to claim 22 and 38 above, and further in view of Kawakita et al. 5,977,490.

EP '405 discloses that via fill material may contain additive to aid in dispersing.

Kawakita et al. teach that conductive paste for filling vias in a circuit board contains dispersant at 0.01-1.5 weight percent to reduce viscosity of the paste so that paste can be filled easily in vias (col. 2, lines 35-38, col. 6, lines 35-42).

It would have been obvious to one of ordinary skill in the art to have modified the method of EP '405 by providing in the via fill material a dispersing agent in the amount in the range of 0.01-1.5 weight%, as taught by Kawakita et al, as provided in via fill conductive paste to reduce viscosity of the paste so that paste can be filled easily in vias.

(8)

Claims 11-18, 20, 22, 27, 32, 34-36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iino et al. 6,207,259.

Iino et al. disclose a method of making a wiring board comprising: filling via-holes in thermosetting insulating substrates with a paste; providing the substrates with copper wiring layers; laminating the substrates; and pressing while heating; The paste can comprise tin powder

and copper powder such that a Cu-Sn intermetallic compound is formed during the heating, organic binder and solvent. The tin powder has average particle diameter of 1-15 microns and the copper powder has average particle diameter of 0.5-5 microns (500-5000 nm). When using tin powder, the heating is not lower than 190°C, preferably not lower than 220°C to promote the formation of the intermetallic compound. Iino et al. disclose using paste comprising 50 wt% copper and 50wt% tin (col. 2-12).

By heat-pressing at preferably not lower than 220°C a laminate containing via-holes filled with a paste of tin powder and copper powder and containing copper wiring to form a copper-tin intermetallic compound in the vias, a solid conductive material is obviously formed in the via-holes including a unified conductive layer and solid phase diffusion layer of either tin or indium and the copper, as claimed.

Further by filling the vias with tin of particle size in the range of 1-15 microns and copper of particle size in the range of 0.5-5 microns, such as 0.5 microns (500 nm), the vias are obviously filled with a metal of relatively large particles and with a metal of relatively fine particles in the range of 1-500 nm, as claimed in Claim 32, and a solid conductive material is obviously formed in the through-holes including a unified conductive layer and solid phase diffusion layer of tin and the copper, as claimed in Claim 28 and 29.

(9)

Claims 23 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iino et al. as applied to claim 22 and 38 above, and further in view of Kawakita et al. 5,977,490.

Kawakita et al. teach that conductive paste for filling vias in a circuit board contains dispersant at 0.01-1.5 weight percent to reduce viscosity of the paste so that paste can be filled easily in the vias (col. 2, lines 35-38, col. 6, lines 35-42).

It would have been obvious to one of ordinary skill in the art to have modified the method of Iino et al. by providing in the via paste a dispersing agent in the amount in the range of 0.01-1.5 weight%, as taught by Kawakita et al, as provided in via fill conductive paste to reduce viscosity of the paste so that paste can be filled easily in vias.

(10)

Claims 11-14, 16-18, 21 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakita et al. 5,977,490.

Kawakita et al. discloses a method of making a circuit board comprising: filling via holes in a thermosetting prepreg with conductive paste; providing the prepreg with copper conductor pattern; laminating prepregs; and heating and pressing. The conductive paste comprises at least one fine grain selected from gold, silver, palladium, copper, nickel, tin and lead of diameter of 0.5-20 microns (500-20000 nm) and surface area of 0.1-1.5 m2/g. Kawakita et al. disclose heating at 180°C and pressing at 50 kg/cm2 (5 MPa) (col. 2-10).

By heat-pressing at 180°C a laminate containing via-holes filled with a paste of tin and copper (as encompassed by using at least one selected from gold, silver, palladium, copper, nickel, tin and lead) and containing copper conductor, a solid conductive material is obviously

formed in the via-holes including a unified conductive layer and solid phase diffusion layer of either tin or indium and the copper, as claimed.

Further by filling the vias with nickel (as encompassed by using at least one selected from gold, silver, palladium, copper, nickel, tin and lead) of particle size in the range of 0.5-20 microns, such as 0.5 microns (500 nm), the vias are obviously filled with a nickel metal of mean particle size in the range of 1-500 nm, as claimed in Claims 28 and 29, and a solid conductive material is obviously formed in the through-holes including a unified conductive layer and solid phase diffusion layer of nickel and the copper, as claimed in Claim 28 and 29.

(11)

Claims 11-14, 16-19, 21, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatakeyama et al. 5,972,482.

Hatakeyama et al. disclose a method of making a circuit board comprising: filling through-holes in a thermosetting resin substrate with a conductive paste; providing the substrate with copper conductive pattern; laminating substrates; and heating under pressure. The temperature during heating is from 170-260°C and the pressure is 20-80 kg/cm2 (2-8 MPa) The metallic particulate of the conductive paste is at least one metal selected from gold, silver, copper, palladium, nickel and an alloy thereof and of average diameter of from 0.2-20 microns (200-20000 nm) (col. 2-6).

By heat-pressing at 170-260°C a laminate containing through-holes filled with a paste of alloy of nickel and copper (as encompassed by using at least one selected from gold, silver, copper, palladium, nickel and alloy thereof) and containing copper conductor, a solid conductive

material is obviously formed in the through-holes including a unified conductive layer and solid phase diffusion layer of nickel and the copper, as claimed in Claim 11.

By heat-pressing at 170-260°C a laminate containing through-holes filled with a paste of nickel of particle size in the range of 0.2-20 microns, such as 0.2 microns (200 nm), the vias are obviously filled with a nickel metal of mean particle size in the range of 1-500 nm, as claimed in Claims 28 and 29, and a solid conductive material is obviously formed in the through-holes including a unified conductive layer and solid phase diffusion layer of nickel and the copper, as claimed in Claim 28 and 29.

Allowable Subject Matter

(12)

Claims 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(13)

Claims 30 and 31 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

(14)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
October 27, 2004